



APPLICATION NO. 09/846.410

TITLE OF INVENTION: Multiple Data Rate Hybrid Walsh Codes
for CDMA

INVENTOR: Urbain A. von der Embse

Clean version of how the CLAIMS will read

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CLAIMS

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WHAT IS CLAIMED IS:

Claim 1. (cancelled)

Claim 2. (cancelled)

15 Claim 3. (cancelled) Claim 4. (cancelled)

Claim 5. (currently amended) A method for implementation of hybrid Walsh complex orthogonal codes for CDMA, said method comprising the steps:

20 generating N Walsh codes $W(c)$ with code index $c=0,1,2,\dots,N-1$,
each with N chips where N is a power of 2,
generating said N hybrid Walsh codes $\tilde{W}(c)$ by re-ordering said
Walsh codes defined by equations

$$\text{for } c = 0, \quad \tilde{W}(c) = W(0) + jW(0)$$

25 $\text{for } c = 1,2,\dots,N/2-1, \quad \tilde{W}(c) = W(2c) + jW(2c-1)$

$$\text{for } c = N/2, \quad \tilde{W}(c) = W(N-1) + jW(N-1)$$

$$\text{for } c = N/2+1,\dots,N-1, \quad \tilde{W}(c) = W(2N-2c-1) + jW(2N-2c)$$

wherein $j=\sqrt{-1}$,

wherein said hybrid Walsh codes are generated by reading code
30 chip values from said Walsh code memory in a digital signal
processor and writing to said hybrid Walsh memories using
addresses specified by said re-orderings of said Walsh
codes and,

applying said hybrid Walsh codes in the encoder and in the decoder by replacing existing said Walsh real codes with said hybrid Walsh complex codes using the same code vector indexing.

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Claim 6. (currently amended) A method for implementation of hybrid Walsh codes for CDMA as described in claim 5, further comprising the steps:

10 using tensor products also called Kronecker products to construct a second code,

wherein an example 24 chip tensor product code is constructed from a 8 chip hybrid Walsh code and a 3 chip discrete Fourier transform DFT code,

15 said 24 chip code is defined by a 24 row by 24 column code matrix C_{24} wherein row vectors are code vectors and column elements are code chips,

said 8 chip hybrid Walsh code is defined by a 8 row by 8 column code matrix \tilde{W}_8 ,

20 said 3 chip DFT code is defined by a 3 row by 3 column code matrix E_3 ;

said C_{24} is constructed by tensor product of said \tilde{W}_8 with said E_3 defined by equation

$$C_{24} = \tilde{W}_8 \otimes E_3$$

25 wherein symbol " \otimes " is a tensor product operation, row $u+1$ and column $n+1$ matrix element $C_{24}(u+1, n+1)$ of said C_{24} is defined by equation

$$C_{24}(u+1, n+1) = \tilde{W}_8(u_0+1, n_0+1) E_3(u_1+1, n_1+1)$$

wherein

30 $u = u_0 + 8u_1$

$$u = 0, 1, \dots, 23$$

$$n = n_0 + 8n_1$$

$$n = 0, 1, \dots, 23$$

wherein u, n are code and chip indices for said codes C_{24} and
 u_0, n_0 are code and chip indices for said code \tilde{W}_8 and u_1, n_1
are code and chip indices for said code E_3 ,
wherein said encoder and said decoder for CDMA communications

5 have memories assigned to said C_{24} , \tilde{W}_8 , E_3 codes,
said C_{24} codes are generated by reading code chip values from said
 \tilde{W}_8 memory and said E_3 memory and combining using said
equations to yield said chip values for said C_{24} codes and
stored in said memory C_{24} ,

10 said C_{24} codes are read from said memory and implemented in said
encoder and said decoder,

using direct products to construct a second code.

wherein an example 11 chip direct product code is constructed
from said 8 chip hybrid Walsh code and said 3 chip DFT
15 code,

said 11 chip code is defined by the 11 row by 11 column code
matrix C_{11} ,

said C_{11} is constructed by direct product of said \tilde{W}_8 with said E_3
defined by equation

20
$$C_{11} = \tilde{W}_8 \oplus E_3$$

wherein symbol " \oplus " is a direct product operation,
row $u+1$ and column $n+1$ matrix element $C_{11}(u+1, m+1)$ of said C_{11} is
defined by equation

$$C_{11}(u+1, n+1) = \tilde{W}_8(u_0+1, n_0+1) \text{ for } u=u_0, n=n_0,$$

25
$$= E_3(u_1+1, n_1+1) \text{ for } u=8+u_1, n=8+n_1,$$

$$= 0 \text{ otherwise,}$$

wherein said encoder and said decoder for CDMA communications

have memories assigned to said C_{11} , \tilde{W}_8 , E_3 codes,

said C_{11} codes are generated by reading code chip values from said
 \tilde{W}_8 memory and said E_3 memory and combined using said
equations to yield said chip values for said C_{11} codes and
stored in said C_{11} memory,

5 said C_{11} codes are read from memory and implemented in said
encoder and said decoder,
using functional combining to construct a second code,
wherein an example 11 chip functional combined \hat{C}_{11} code is
10 constructed from said C_{11} codes by using codes to fill the
two null subspaces of said C_{11} .
wherein said \hat{C}_{11} codes are read from memory and implemented in
Said encoder and said decoder and,
using a combinations of tensor products, direct products, and
15 functional combining to construct said codes which are
read from memory and implemented in said encoder and
said decoder.

15 Claim 7. (currently amended) A method for implementation of
Hybrid Walsh codes for CDMA, further comprising the steps:
said encoder operates as a block encoder,
encoding blocks of received N data symbols with said N hybrid
Walsh codes and summing to yield N chips for each block at
20 the output chip rate $1/T$ chips per second,
wherein said encoder accepts up to M users per block for $N=2^M$,
said users have data rates from the menu $1/NT, 2/NT, \dots, 2/T$
respectively corresponding to $1, 2, \dots, N/2$ said user
data symbols over said block,
25 user data symbols over said block are arranged in packets with
each packet containing said user data symbols for said
block,
said encoder accepts packets from each user and writes them to
memory "A" for each block,
30 binary address index $d=d_0+2d_1+4d_2+\dots+(N/2)d_{M-1} = 0, 1, \dots, N-1$ is
used for addressing of said data symbols stored in "A"
wherein binary coefficients d_0, d_1, \dots, d_{M-1} take values
0, 1,
said binary address index can be independently mapped onto said

data symbol addresses of "A" to provide additional flexibility in assigning users to hybrid Walsh vectors, said data symbol address is partitioned into M overlapping algebraic index fields d_{M-1} , $d_{M-2}d_{M-1}, \dots, d_1d_2 \dots d_{M-2}d_{M-1}$,
5 $d_0d_1d_2 \dots d_{M-2}d_{M-1}$, with each field indexed over the allowable number 2, 4, . . ., $N/2, N$ of said data rate users at symbol rates $1/2T, 1/4T, \dots, 2/NT, 1/NT$ respectively,
assign said users with like data symbol rates to the M groups
10 $u_0, u_1, \dots, u_{M-2}, u_{M-1}$, of users with the respective symbol rates $1/2T, 1/4T, \dots, 2/NT, 1/NT$,
assign said data symbol indices in said index field d_{M-1} to said users in said group u_0 , assign said data symbol indices in said index field $d_{M-2}d_{M-1}$ to said users in said group u_1 , et
15 al and finally assign said data symbol indices in said index field $d_0d_1d_2 \dots d_{M-2}d_{M-1}$ to said users in said group u_{M-1} , use said mapping and assignments to specify said write addresses of said user data symbols onto said input code vector stored in said memory "A" and,
said input vector in said "A" is encoded in said encoder and
20 processed for transmission.

Claim 8. (currently amended) Wherein said hybrid Walsh codes in claim 5 have a fast encoding implementation algorithm,
25 comprising the steps:
said fast implementation algorithm in encoder uses said memory "A" for input and to support pass 1, memories "B", "C" to support passes 2, . . ., M and re-ordering pass, and memory "D" for output,
30 write input data symbol vector $Z(d_0, d_1, \dots, d_{M-2}, d_{M-1})$ to said "A" wherein said $(d_0, d_1, \dots, d_{M-2}, d_{M-1})$ is said binary addressing index after said mapping of said data vector onto said "A",
pass 1 reads from said "A", performs pass 1, and writes the

output to said "B",
 pass 1 multiplies said Z by the kernel $[(-1)^{dr_0n_{M-1}} + j(-1)^{di_0n_{M-1}}]$ and sums over $dr_0, di_0 = 0, 1$ to yield the partially encoded symbol set $Z(n_{M-1}, d_1, \dots, d_{M-2}, d_{M-1})$ where $dr_0 = cr(d_0)$ and $cr(d)$ is the real axis Walsh code for d , $di_0 = ci(d_0)$ where $ci(d)$ is the imaginary axis Walsh code for d , and n_{M-1} is a binary code chip coefficient in said code chip indexing $n = n_0 + 2n_1 + \dots + (N/4)n_{M-2} + (N/2)n_{M-1}$,
 5 write said output symbol set $Z(n_{M-1}, d_1, \dots, d_{M-2}, d_{M-1})$ to said "B" wherein said address index n_{M-1} replaces said index d_0 ,
 10 pass 2 reads from said "B", performs pass 2, and writes the output to said "C",
 pass 3 reads from said "C", performs pass 3, and writes the output to said "B",
 15 subsequent passes alternate in read/write from/to said "B" and write/read to/from said "C",
 implement passes $m=2, 3, \dots, M-1$ of said fast encoding algorithm by multiplying
 $Z(n_{M-1}, n_{M-2} \dots, n_{M-m+1}, d_{m-1}, \dots, d_{M-2}, d_{M-1})$ by the kernel
 20 $[(-1)^{dr_{m-1}(n_{M-m} + n_{M-m+1})} + j(-1)^{di_{m-1}(n_{M-m} + n_{M-m+1})}]$ and summing over $dr_{m-1}, di_{m-1} = 0, 1$ to yield the partially encoded symbol set $Z(n_{M-1}, n_{M-2} \dots, n_{M-m}, d_m, \dots, d_{M-2}, d_{M-1})$,
 implement pass M of said fast encoding algorithm by
 25 by multiplying $Z(n_{M-1}, n_{M-2} \dots, n_2, n_1, d_{M-1})$ by the kernel $[(-1)^{dr_{M-1}(n_0 + n_1)} + j(-1)^{di_{M-1}(n_0 + n_1)}]$ and summing over $dr_{M-1}, di_{M-1} = 0, 1$ to yield the encoded symbol set
 $Z(n_{M-1}, n_{M-2} \dots, n_2, n_1, n_0)$,
 reorder said encoded symbol set in memory in the ordered output format $Z(n_0, n_1, \dots, n_{M-2}, n_{M-1})$ and store in said "D" and,
 30 said encoder in said transmitter reads said encoded symbol vector in said "D" and overlays said vector with long and short PN codes to generate N chips of said hybrid Walsh encoded data symbol vector for subsequent processing and transmission.

Claim 9. (currently amended) Wherein said hybrid Walsh codes in claim 5 have a fast decoding implementation algorithm, comprising the steps:

- 5 said decoder in said receiver strips off said PN codes from said received N chip encoded data symbol vector and outputs said received hybrid Walsh encoded chip vector $Z(n_0, n_1, \dots, n_{M-2}, n_{M-1})$ for implementation of said fast decoding algorithm,
- 10 said fast implementation algorithm in said decoder uses memory "E" for input and to support pass 1, memories "F", "G" to support passes 2, 3, . . . , M and re-ordering pass, and memory "H" for output,
write said $Z(n_0, n_1, \dots, n_{M-2}, n_{M-1})$ to said "E" wherein $(n_0, n_1, \dots, n_{M-2}, n_{M-1})$ is the binary address,
- 15 pass 1 reads from said "E", performs pass 1, and writes the output to said "F",
implement pass 1 of said fast decoding algorithm by multiplying said $Z(n_0, n_1, \dots, n_{M-2}, n_{M-1})$ by the kernel $[(-1)^{n_0 dr_{M-1} + j} (-1)^{n_0 di_{M-1}}]$ and summing over $n_0=0,1$ to yield the partially decoded symbol set
 $Z(d_{M-1}, n_1, \dots, n_{M-2}, n_{M-1}),$
write said output symbol set $Z(d_{M-1}, n_1, \dots, n_{M-2}, n_{M-1})$ to said "F" wherein address index d_{M-1} replaces index n_0 ,
- 20 pass 2 reads from said "F", performs pass 2, and writes the output to said "G",
pass 3 reads from said "G", performs pass 3, and writes the output to said "F",
subsequent passes alternate in read/write from/to said "F" and
- 25 write/read to/from said "G",
implement passes $m=2, 3, \dots, M-1$ of said fast decoding algorithm by multiplying $Z(d_{M-1}, d_{M-2}, \dots, d_{M-m+1}, n_{m-1}, \dots, n_{M-2}, n_{M-1})$ by the kernel $[(-1)^{n_{m-1} (dr_{M-m} + dr_{M-m+1}) + j} (-1)^{n_{m-1} (di_{M-m} + di_{M-m+1})}]$ and summing over $n_{m-1}=0,1$ to yield the partially decoded symbol set

$Z(d_{M-1}, d_{M-1}, d_{M-2}, \dots, d_{M-m}, n_m, \dots, n_{M-2}, n_{M-1})$,
implement pass M of said fast decoding algorithm by
by multiplying $Z(d_{M-1}, d_{M-2}, \dots, d_2, d_1, n_{M-1})$ by the kernel
 $[(-1)^{n_{M-1}}(dr_0 + dr_1) + j(-1)^{n_{M-1}}(di_0 + di_1)]$ and summing over
5 $n_{M-1}=0,1$ and rescaling by dividing by $2N$ to yield the
decoded symbol set
 $Z(d_{M-1}, d_{M-1}, d_{M-2}, \dots, d_2, d_1, d_0)$,
reorder said decoded symbol set in the ordered output format
 $Z(d_0, d_1, \dots, d_{M-2}, d_{M-1})$ and store in said "H" and,
10 said decoder in said receiver reads said decoded symbol vector
in "D", re-orders the read data symbols to remove said
mapping onto said "A", and performs subsequent receive
signal processing to recover the information from the
data symbols..

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